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Citation for final published version:

Han, Yu, Li, Qiang ORCID: <https://orcid.org/0000-0002-5257-7704> and Lau, Kei May 2017. Tristate memory cells using double-peaked fin-array III-V tunnel diodes monolithically grown on (001) silicon substrates. IEEE Transactions on Electron Devices 64 (10) , pp. 4078-4083. 10.1109/TED.2017.2738675 file

Publishers page: <http://dx.doi.org/10.1109/TED.2017.2738675>  
<<http://dx.doi.org/10.1109/TED.2017.2738675>>

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# Tri-state memory cells using double-peaked fin-array III-V tunnel diodes monolithically grown on (001) silicon substrates

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**Abstract**— We demonstrate functional tri-state memory cells using multi-peaked GaAs/InGaAs fin-array tunnel diodes grown on exact (001) Si substrates. On-chip connection of single-peaked tunnel diode arrays produces I-V characteristics with multiple negative-differential resistance regions. We designed and fabricated two types of tri-state memory cells. In one design, a double-peaked tunnel diode was used as the drive, and a reverse-biased single-peaked tunnel diode as the load. In the other design, the tri-state memory cell was realized by series connection of two forward-biased single-peaked tunnel diodes.

**Index Terms**—multi-valued logic, tunnel diodes, memory cell, GaAs fin-array

## I. INTRODUCTION

As CMOS scaling approaches atomistic and quantum mechanical boundaries, excessive power dissipation and severe RC degradation are becoming more and more pressing issues in present-day binary logic systems [1]. Multi-valued logic can potentially overcome these bottlenecks by enhancing signal encoding efficiency and reducing interconnection complexity [2]. Compared with bistable Si MOSFETs, tunnel diodes with negative-differential resistance (NDR) are preferred building blocks for multi-valued logic systems [3]-[6]. The pico-second switching characteristics of tunnel diodes also favors ultra-high speed circuit design [7]. Although Si-based resonant inter-band tunneling diodes and multi-valued logic circuitry have been developed [8], III-V based tunnel diode-transistor circuits can potentially deliver superior performance because of the direct bandgap and smaller tunneling mass [9]. Unfortunately, integrating high performance III-V tunnel diodes onto mainstream (001) Si substrates is challenging due to the large lattice and thermal mismatches. Attempts to grow III-V tunnel diodes on Si usually rely on thick buffer layers to reduce defect density [10]-[14]. Recently, growing III-V nanostructures (including GaAs, InP, InGaAs, InAs and GaSb) on Si utilizing the aspect ratio trapping (ART) technique in realizing high crystalline

quality III-V buffers within a few tens of nanometers has been demonstrated [15]-[22]. Previously, we have reported on the use of III-V FinFET on Si technology to demonstrate GaAs/InGaAs fin-array tunnel diodes and monolithically integrated digital circuits [23]-[25]. Here, we demonstrate the use of the tunnel diode arrays to create tri-state memory cells. Multi-peaked tunnel diodes were realized via on-chip connection of single-peaked tunnel diodes electrically isolated by SiO<sub>2</sub> spacers. Combining single-peaked and double-peaked tunnel diodes under forward and reverse-biases, we demonstrate functional tri-state memory cells on CMOS-compatible on-axis (001) silicon substrates. Compared with traditional CMOS based binary memories, these tri-state memory cells using III-V tunnel diodes could potentially lead to reduced power dissipation, improved operation speed and high integration density [26]-[30].

## II. GALLIUM ARSENIDE FIN-ARRAY ON SILICON

The experiment started with the growth of GaAs fins on patterned (001) Si substrates by metal-organic chemical vapor deposition (MOCVD) [23]. V-grooved pockets were formed by anisotropic KOH wet etching. Fig. 1(a), presenting a 70° tilted-view scanning electron microscope (SEM) image of the as-grown sample, reveals highly ordered GaAs fin-array with two convex (111) facets. Cross-sectional transmission electron microscope (TEM) image of one GaAs fin is displayed in Fig. 1(b). Most of the defects are confined within an ultra-thin nucleation layer at the GaAs/Si interface, resulting in good material quality at the junction region. The tunnel junction consists of, from bottom to top, 150 nm thick carbon doped p-GaAs ( $3.8 \times 10^{19} \text{ cm}^{-3}$ ), 5 nm n-In<sub>0.2</sub>Ga<sub>0.8</sub>As and 80 nm silicon doped n-GaAs ( $> 1.0 \times 10^{19} \text{ cm}^{-3}$ ). We calibrated the carrier concentration by Hall measurement using thin films on GaAs substrates under the same growth conditions. Fig. 1(c) illustrates the band diagram of the tunnel diode showing the effect of inter-band tunneling through the thin pseudomorphic InGaAs layer. We calculated the Fermi levels for the highly doped n- and p-GaAs inside the conduction/valance band using the following equations [31]:

$$qV_n = kT \left\{ \ln\left(\frac{n}{N_C}\right) + 2^{-3/2} \left(\frac{n}{N_C}\right) \right\} \quad (1)$$

$$qV_p = kT \left\{ \ln\left(\frac{p}{N_V}\right) + 2^{-3/2} \left(\frac{p}{N_V}\right) \right\} \quad (2)$$

Manuscript received 2017; revised xxx. This work was supported by a grant (16245216) from the Research Grants Council, and by Innovation Technology Fund (ITS/320/14) of Hong Kong. The review of this letter was arranged by Editor xx.

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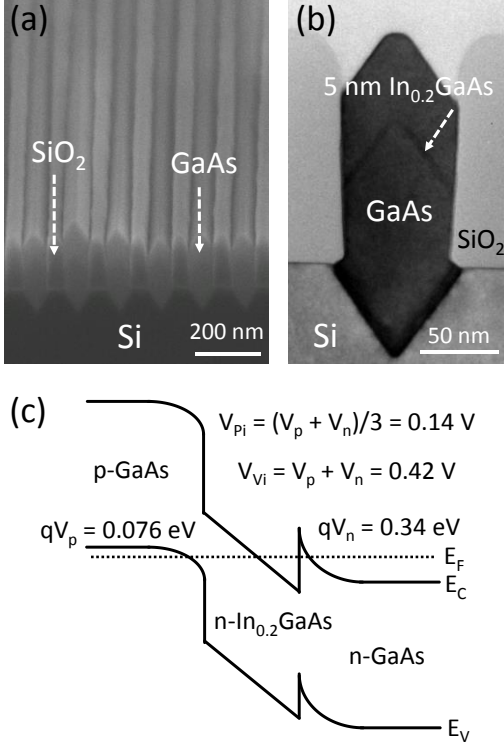


Fig. 1. (a) 70° tilted view SEM image of the as-grown highly-ordered GaAs fins on Si. (b) Cross-sectional TEM image of the tunnel diode, showing defect confinement inside the V-groove and the 5 nm In<sub>0.2</sub>Ga<sub>0.8</sub>As interlayer. (c) Band diagram of the tunnel junction. Degeneracy of the junction is calculated and labeled.

$V_n$  and  $V_p$  are the amount of degeneracy of n-GaAs and p-GaAs, respectively.  $N_C$  and  $N_V$  refer to the effective density of states of the conduction and valance band, while  $n$  and  $p$  represent the doping levels of the n-GaAs and the p-GaAs regions. At room temperature,  $V_p$  is 0.076 V and  $V_n$  is 0.34 V, based on the calibrated carrier concentrations. The huge difference of  $V_n$  and  $V_p$  mainly stems from the difference of  $N_C$  ( $4.7 \times 10^{17} \text{ cm}^{-3}$ ) and  $N_V$  ( $9.0 \times 10^{18} \text{ cm}^{-3}$ ). The intrinsic peak voltage ( $V_{Pi}$ ) refers to the bias necessary to align the maximum electron density to the maximum hole density, while the intrinsic valley voltage ( $V_{Vi}$ ) is the bias to align the conduction band minimum with the valance band maximum. We estimated both  $V_{Pi}$  and  $V_{Vi}$  using equation (3) and (4) from Ref. [32].  $V_{Pi}$  is around 0.14 V and  $V_{Vi}$  is about 0.42 V.

$$V_{Pi} = (V_n + V_p)/3 \quad (3)$$

$$V_{Vi} = (V_n + V_p) \quad (4)$$

### III. DEVICE FABRICATION

Fig. 2 presents the process flow and schematic of the fabricated double-peaked tunnel diodes and tri-state memory cells. Device fabrication started with the activation of hydrogen passivated carbon in the p-GaAs at 550 °C for 30 sec under N<sub>2</sub> ambient. Then, Ni/Ge/Au metal stack was patterned onto the exposed n-GaAs fins. We used wet etching (H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O = 3:1:50) to remove the top n-GaAs/In<sub>0.2</sub>Ga<sub>0.8</sub>As layer and stop at the p-GaAs layer in the

unmasked region. Note that tunnel diodes occupying different trenches were electrically isolated by the SiO<sub>2</sub> spacers. Even though leakage current through the n-Si substrate exists, the amount is negligible compared with the peak current of the tunnel diodes. This feature allows us to achieve on-chip interconnection of individual tunnel diodes in parallel fins. Fig. 3 displays the equivalent circuit of the fabricated devices, with five tunnel diodes connected through four different ports.  $R_C$  corresponds to the contact resistance between the metal stack and the n-GaAs fins and  $R_W$  refers to the resistance of the partially etched p-GaAs fins. Table I summarizes the circuit functions when probing different metal pads.

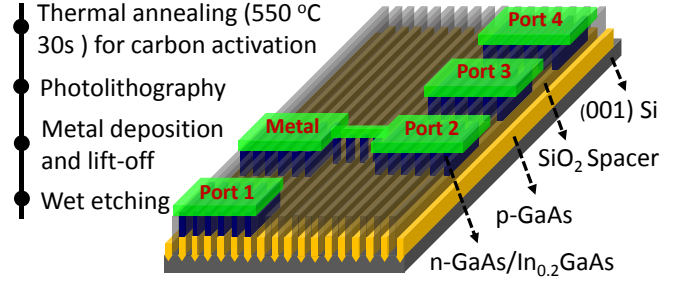


Fig. 2. Process flow and schematic of the double-peaked tunnel diode and the tri-state memory cells. The size of the electrodes is  $100 \times 100 \mu\text{m}^2$ .

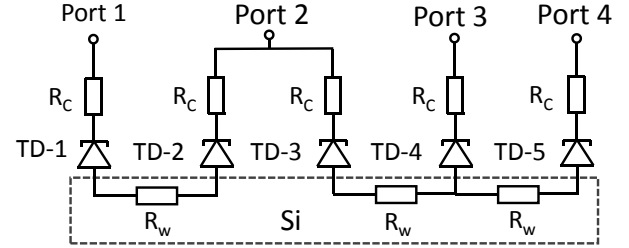


Fig. 3. Equivalent circuit of the fabricated double-peaked tunnel diodes and the tri-state memory cells.

TABLE I  
SUMMARY OF THE CIRCUIT FUNCTIONS WHEN PROBING DIFFERENT METAL PADS

Apply voltage	Ground	Measured voltage	Function
Port 3	Port 4	NA	Single peak TD
Port 1	Port 3	NA	Double peak TD
Port 1	Port 4	Port 3	Memory cell (load resistor)
Port 4	Port 1	Port 2	Memory cell (Load TD)

### IV. DOUBLE-PEAKED FIN-ARRAY TUNNEL DIODES

To measure the I-V characteristics of single-peaked tunnel diodes, double sweep from  $-1.5$  V to  $1.5$  V and  $1.5$  V to  $-1.5$  V were applied on Port 3, with Port 4 grounded. With two tunnel junctions connected back to back, at any measurement point, one tunnel diode was forward biased and the other was reverse biased (behaving like a resistor). As a result, we observed symmetric NDR regions as shown in Fig. 4(a). Due to the parasitic resistance, both peak and valley voltage is larger than the intrinsic values. Besides, since the value of parasitic resistance is larger than that of NDR, hysteresis is observed under the double sweep condition and



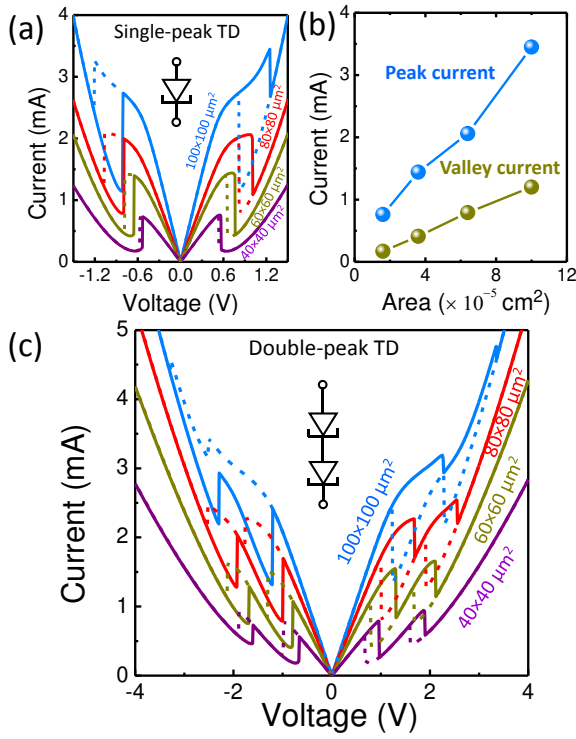


Fig. 4. (a) IV characteristic of single-peaked tunnel diodes with different sizes. Solid curves refer to sweeping forward and dotted curve sweeping backward. (b) The linear scaling of peak current and valley current with device sizes. (c) IV characteristic of double-peaked tunnel diodes with different sizes. Solid curves refers to sweeping forward and dotted curves sweeping backward.

aggravates as device size increases due to unmatched scaling of NDR and the contact resistance. Fig. 4(b) indicates the linear scaling of peak current and valley current with device size. When measuring the IV characteristic at Port 3 with Port 1 grounded, a double-peaked tunnel diode was formed by the series connection of two single-peaked tunnel diodes. At either forward or reverse bias, two tunnel diodes were forward biased and the other two reverse biased. The measured curves are shown in Fig. 4(c). We observed double-peaked characteristic and hysteresis in all the measured devices.

## V. DOUBLE-STATE MEMORY CELLS

We firstly fabricated a two-state memory cell to illustrate the working principle of tunnel diode based memory circuits. Fig. 5 (a) shows the schematic of a two-state memory cell using one forward-biased single-peaked tunnel diode as drive and another reverse-biased counterpart (serving as a resistor) as load. Detailed electrical analysis of this structure can be found in Ref. [24] and [25]. Fig. 5(b) presents the load line analysis. With a properly selected static input voltage  $V_{\text{static}}$ , two stable working points (Q1 and Q2) can be realized. This bi-stable condition can only be obtained when the value of load resistance exceeds that of the NDR. These working states (Q1 and Q2) could be regarded as stored digital values inside a memory cell. Changing the working points requires a writing-pulse at the input end. A sudden increase of the write-voltage would move the load line to pass through the peak of the tunnel diode and the subsequent return to the  $V_{\text{static}}$  would shift

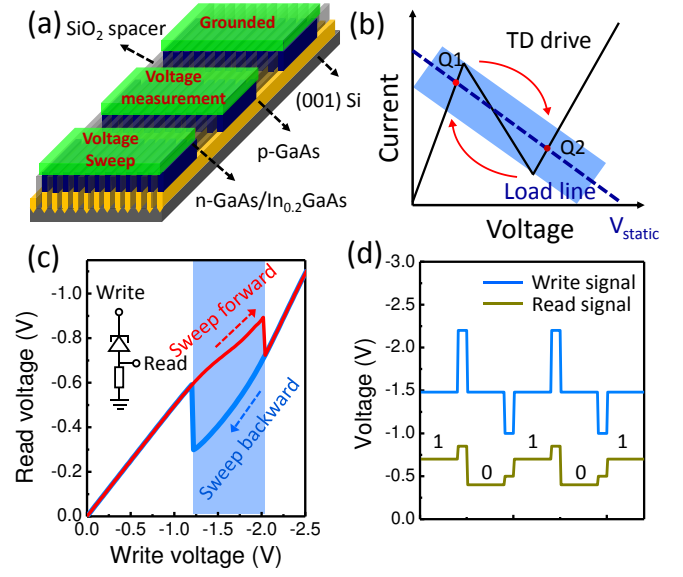


Fig. 5. (a) Schematic of the double-state memory cell. (b) Load line analysis showing the basic principle of a two-state memory cell composed of a single-peaked tunnel diode connected with a resistor. Shaded area indicates double-states. (c) Measured output (read) voltage of the load resistor when sweeping the write voltage forward and backward. Shaded area indicates double states. (d) Waveforms showing the function of the two-state memory cell at static write-voltage of -1.48 V. Writing pulses change the stored value.

the working point to Q2. The switching of the working points could be illustrated more clearly in Fig. 5 (c), plotting the measured output (read) voltage across the load resistor when sweeping the input (write) voltage forward and backward. When sweeping forward, the read-voltage increased linearly with the write-voltage and then underwent a sudden slump when the write voltage approached  $-2.02 \text{ V}$ . This reveals the transition from the bi-stable condition to the mono-stable condition as indicated by the upper red arrow in Fig. 5(b). Similarly, when sweeping backward, an abrupt jump of read-voltage occurred as the write-voltage approached  $-1.22 \text{ V}$  (corresponding to the lower red arrow in Fig. 5(b)). For any write-voltage falling between  $-1.22 \text{ V}$  to  $-2.02 \text{ V}$ , there are two possible read-voltages as indicated by the blue shaded regions. The two stable read-voltages corresponds to the working points (Q1 and Q2) shown in Fig. 5(b). For an initial state Q1, a write-pulse smaller than  $-2.02 \text{ V}$  would shift the circuit from bi-stable to mono-stable condition and then to state Q2. Analogously, for an initial state Q2, a write-pulse larger than  $-1.22 \text{ V}$  would shift the working point to Q1. For example, with an initial stored voltage of  $-0.7 \text{ V}$ , a writing pulse of  $-2.2 \text{ V}$  would change the stored value to  $-0.4 \text{ V}$  while a  $-1 \text{ V}$  pulse moves the state back to  $-0.7 \text{ V}$ . The corresponding waveforms illustrating the state-changing function is presented in Fig. 5(d). The ranges of the voltage for the stored digital values ("0" and "1") are:  $-0.30 \text{ V}$  to  $-0.72 \text{ V}$ , and  $-0.59 \text{ V}$  to  $-0.89 \text{ V}$ , respectively. The noise margin of each state could be defined as the minimum value of the voltage difference between the operating point and the minimum of the read-voltage, and the voltage difference between operating point and the maximum of the read voltage [33]. Thus, at a static write-voltage of  $-1.48 \text{ V}$ , a noise margin of  $0.10 \text{ V}$  and  $0.11 \text{ V}$  is extracted for states "0" and "1", respectively.

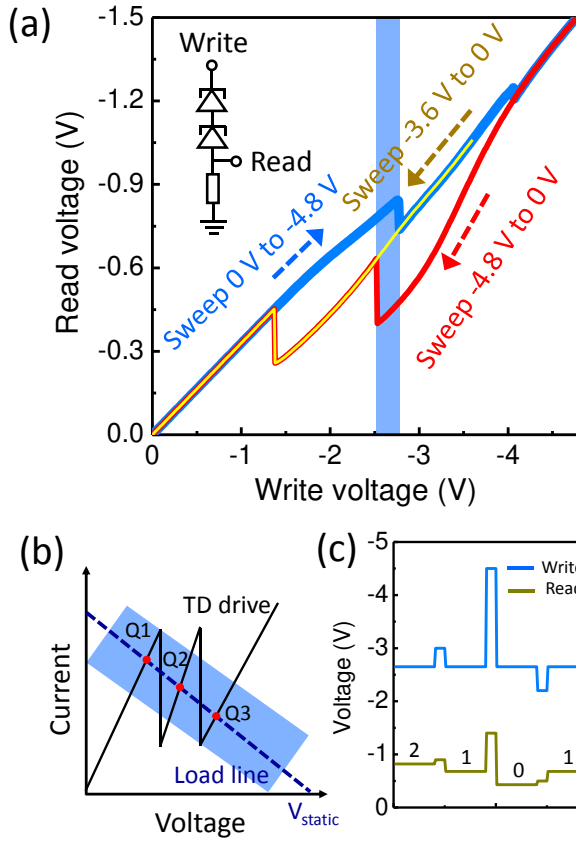


Fig. 6. (a) Measured output (read) voltage of the load resistor when sweeping the write-voltage forward and backward. Shaded area indicates tri-states. (b) Load line analysis showing the basic principle of tri-state memory cells based on double-peaked tunnel diodes. Shaded area indicates tri-states. (c) Waveforms showing the function of the tri-state memory cell at  $-2.65$  V static write voltage.  $-0.82$  V,  $-0.68$  V and  $-0.43$  V refers to logic states “2”, “1” and “0” respectively.

## VI. TRI-STATE MEMORY CELLS

A tri-state memory cell was then built by applying the write-voltage at Port 1 and extracting the read-voltage from Port 3 in Fig. 2 and Fig. 3. Voltage sweep from 0 to  $-4.8$  V,  $-4.8$  V to 0 V and  $-3.6$  V to 0 V was applied on Port 1, with Port 4 grounded. Fig. 6(a) presents the relationship of the read-voltage and the write-voltage under different sweeping conditions. Single-valued read-voltage is observed when the write-voltage is larger than  $-1$  V or smaller than  $-4$  V. Two possible read-voltages are obtained when the write-voltage falls between  $-1.38$  and  $-2.53$  V or  $-2.76$  and  $-4.06$  V. For write-voltage ranging from  $-2.53$  V to  $-2.76$  V, we observed a tri-state output region with one write-voltage corresponding to three possible read-voltages as highlighted by the blue shade. The mechanism of this multi-valued output is explained as follows. A tri-state memory cell can be built by connecting a double-peaked tunnel diode with a load resistor. When applying a negative voltage at Port 1 with Port 4 grounded, both TD-1 and TD-3 were forward biased (serving as single-peak tunnel diode), and TD-2 and TD-5 were reversed biased (serving as resistor). The series connection of TD-1 and TD-3 formed a double-peaked tunnel diode and the reversed biased TD-5 served as load resistor. The load line analysis in Fig. 6(b) indicates the basic working principle of this tunnel diode based tri-state memory cell. Three stable working

TABLE II.  
THE VALUE OF WRITING PULSE REQUIRED FOR CHANGING THE STORED LOGIC STATES.

Value change	Writing pulse (V)
$0 \rightarrow 1$	$-2.53 < V < -1.38$
$0 \rightarrow 2$	$V > -1.38$
$1 \rightarrow 0$	$V < -4.06$
$1 \rightarrow 2$	$V > -1.38$
$2 \rightarrow 0$	$V < -4.06$
$2 \rightarrow 1$	$-4.06 < V < -2.76$

points (Q1, Q2 and Q3) can be clearly detected when selecting a proper load resistance and a static write-voltage. Each working point can be regarded as a stored digital value and the stored value can be altered by a writing pulse at the input end. Given an initial working point of Q1, a small writing pulse would move the load line to pass through the first peak of the double-peaked tunnel diode and then return to the working point of Q2. Similarly, a large writing-pulse would move the load line to pass through the second peak and then return to the working point of Q3. For example, given a write-voltage of  $-2.65$  V and an initial stored voltage of  $-0.82$  V (regarded as digit “2”), applying a pulse between  $-2.76$  V and  $-4.06$  V would change the stored value to  $-0.68$  V (regarded as digit “1”). Similarly, another pulse smaller than  $-4.06$  V would change the stored value further to  $-0.43$  V (regarded as digit “0”). The ranges of voltage for different states “0”, “1” and “2” extracted from Fig. 6(a) are:  $-0.49$  V to  $-0.40$  V,  $-0.74$  V to  $-0.63$  V, and  $-0.84$  V to  $-0.78$  V, respectively. At a static write-voltage of  $-2.65$  V, a noise margin of 30 mV, 50 mV and 20 mV could be extracted for states “0”, “1” and “2”. The noise margin of this tri-state memory cell is determined by the first peak and second valley of the double-peaked tunnel diode, as bounded by the edges of the blue shade in Fig. 6(b). Larger noise margin could be obtained by improving the peak current density and the PVCRR of the double-peaked tunnel diode. Fig. 6(c) presents the waveforms of the writing and the reading functions and Table II summarizes the write-pulses necessary to alter the stored values.

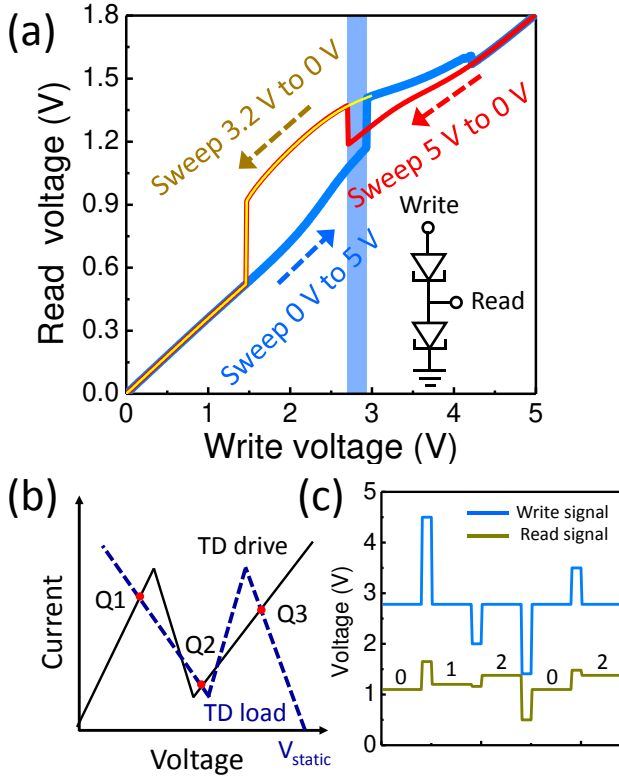


Fig. 7. (a) Measured output (read) voltage of the load tunnel diode when sweeping the write-voltage forward and backward. Shaded area indicates tri-states region. (b) Load line analysis showing the basic principle of the tri-state memory cell based on tandem single-peaked tunnel diodes. (c) Waveforms showing the functions of the tri-state memory cell at 2.78 V static write voltage. 1.38 V, 1.20 V and 1.10 V refer to logic states “2”, “1” and “0” respectively.

Another type of tri-state memory cell was realized using a different connection method. Shown in Fig. 7(a) are voltage sweeps from 0 to 5 V, 5 V to 0 V and 3 V to 0 V applied at Port 4 with Port 1 grounded and the read-voltage was measured at Port 2 (see schematics in Fig. 2 and Fig. 3). For the write-voltage falling between 2.71 V and 2.93 V, we detected three possible read-voltages within the shaded region. During the measurement, TD-1 and TD-3 were forward biased and TD-2 and TD-5 were reversed biased. This configuration can be simplified as two tandem single-peaked tunnel diodes. The measured read voltage was thus the voltage drop at one forward-biased single-peaked tunnel diode. As indicated by the load line analysis in Fig. 7(b), three stable working points (Q1, Q2 and Q3) could be realized at the intersection of the positive differential resistance regions of the two single-peaked tunnel diodes. These three different working points can be seen as stored digital values of the memory cell. Changing the stored values requires a writing-pulse. Note that, the switching sequence of the working points in the load line analysis depends on the peak current difference of the drive and load tunnel diodes, which may result from process non-uniformity. The most efficient and clear method to determine the switching sequence is through the measurement presented in Fig. 7(a). Details of the three working points and writing-pulses can be precisely extracted. For example, as shown in Fig. 7(c), the stored value changes from “0” to “1” and then to “2”, when a 4.5 V pulse and a subsequent 2.0 V pulse are

applied. The voltage ranges for different states “0”, “1” and “2” are: 1.07 V to 1.17 V, 1.18 V to 1.26 V, and 1.37 V to 1.41 V, respectively. Given a static write-voltage of 2.78 V, we can determine the noise margin of states “0”, “1” and “2” as 30 mV, 20 mV and 10 mV. As shown in Fig. 7(b), the noise margin of this tri-state memory cell is closely associated with the peak voltage, valley voltage and projected peak voltage (has same current value with the peak voltage in the IV curve) of the load/drive tunnel diodes. Expansion of the tri-state region is possible through increasing the voltage swing (voltage difference between the peak voltage and projected peak voltage) of the tunnel diodes. We summarize the values of the writing pulses necessary to alter the stored digits in Table III.

TABLE III.  
THE VALUE OF WRITING PULSE REQUIRED FOR CHANGING THE STORED LOGIC STATES.

Value change	Writing pulse (V)
0 $\rightarrow$ 1	$V > 4.21$
0 $\rightarrow$ 2	$2.93 < V < 4.21$
1 $\rightarrow$ 0	$V < 1.47$
1 $\rightarrow$ 2	$1.47 < V < 2.71$
2 $\rightarrow$ 0	$V < 1.47$
2 $\rightarrow$ 1	$V > 4.21$

## VII. CONCLUSION

In conclusion, we have demonstrated two types of tri-state memory cells using doubled-peaked GaAs/InGaAs fin-array tunnel diodes grown on exact (001) Si substrates by selective epitaxy. The stored digital states of the memory cells can be controlled by the writing pulses and the pulse value determines the next transition state. These results show promises for realizing III-V tunnel diode based multi-valued logic systems on Si substrates.

## ACKNOWLEDGMENT

We thank SEMATECH for providing the initial patterned Si substrates and the NFF and MCPF of HKUST for technical support.

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